A Sensing Circuit For Micro-Capacitance Tomography

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Abstract – *A circuit is described that has applications for micro scale capacitance tomography. The circuit has been developed for use with linear arrays of rectangular electrodes measuring between 10㎜m-100㎜m and integrated onto a silicon chip.*
Simulations suggest that the circuit is capable of measuring very small capacitance changes of the order of tens of atto-farads. The circuit also features a small area footprint, which allows the implementation of large arrays of electrodes, and the associated measurement circuitry, onto one integrated circuit.

Keywords: Capacitance, Measurement, VLSI, Micro-Tomography

1 INTRODUCTION

Electrical capacitance tomography is enjoying considerable success for interrogating industrial processes [1]. Almost all applications to date have involved measurements on a macro scale, typically of the order of centimetres. However, there is potential to exploit the technique for determining process parameters at a much smaller scale, of the order of microns. To achieve this order of spatial resolution will require small sensors and equally small electronic measurement circuitry. The natural candidate for implementing such sensors is silicon integrated circuit technology. Possible applications for micro scale tomographic measurement would be for examining bubble formation and particle sizing in powders. Related developments are being pursued using electrical resistance tomography at the University of Exeter [2].

Section 2 will discuss the requirements of a micro capacitance tomography system from the point of view of sensors, and the measurement circuitry to monitor these sensors. Section 3 describes the types of circuit that have been considered for capacitance measurement, and a description of the chosen circuit is given in section 4. Finally, section 5 presents suggestions on how this circuit could be applied to create a tomographic system.

2 REQUIREMENTS

It seems likely that micro-capacitance tomography will present distinctly different challenges to a macro scale system. Both sensors and measurement circuitry will be integrated onto the same piece of silicon, as it is not practical to implement a micro-tomography system with discrete circuitry. The stray capacitance on a PCB track would be several orders of magnitude greater than any sensor capacitance, and would entirely swamp any capacitance being measured.

Integrating measurement circuitry in close proximity to the sensors should reduce the effects of stray capacitance to a minimum, hence making a system practical. However, it is likely that the capacitances being measured will be very small, possibly of the order of femto-farads. Additionally, due to current limitations of silicon processing, the system will be inherently planar. This presents new challenges both in terms of sensor design and image reconstruction.

2.1 Likely Capacitance of Sensors

Possible electrode configurations have been investigated with Maxwell 3D, a finite element analysis software package produced by Ansoft.

The size and shape of any electrodes produced on silicon are subject to a stringent set of design rules provided by the manufacturer. A CMOS process consists of a large number (20 or more) of layers. These layers define features such as metalisation, contact holes and regions of doping. The design rules govern the relative size, spacing and overlap of all the various layers.

The latest, state of the art digital CMOS processes can produce a minimum feature size of 0·18μm with analogue processes tending to be slightly larger. In most cases, the minimum metal track width, and the minimum track separation, will be greater than the minimum feature size by a factor of two or more. Additionally, these very small processes are very

expensive. Cheaper alternatives are available with a minimum feature size of 0·5μm.

The thickness of a metal track is a parameter that is not under the control of the designer, but rather is a function of the manufacturing process. The thickness will typically be 1μm or less.

A protective passivation layer covers most metal tracks on silicon. This is a further parameter that needs consideration. The passivation layer will usually be made of silicon oxide or silicon nitride, will typically be 1μm or less in thickness, and may optionally be removed from certain areas in some processes. The passivation layer does not form a uniform surface. At a micrometre scale, the surface undulates depending on the layers below it.

Several electrode configurations have been simulated, with due care taken to ensure that these configurations represent a realistic structure that could be achieved in silicon. An example of the type of configuration simulated is shown in Figure 1.

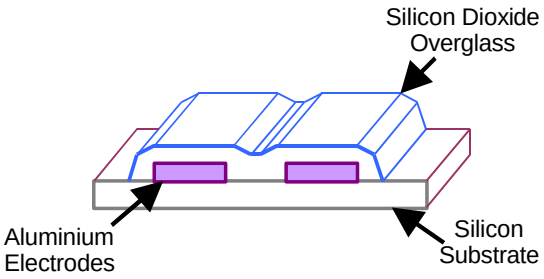

Figure 1: A typical electrode configuration

Two scanning electron microscope images of a sensor integrated on a 0.8μm process are shown in Figure 2. The left-hand image shows a sensor with a layer of glass, and the right-hand image a sensor with the glass removed.

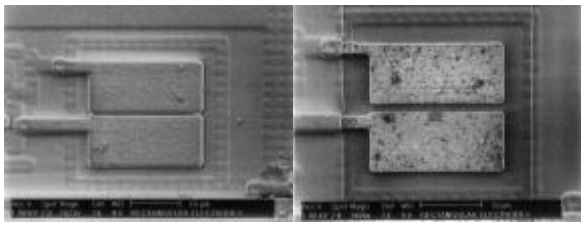

Figure 2: SEM of a Prototype Sensor (21.6μm squares)

Typical structures simulated have been squares measuring between 10μm and 20μm. When simulated, it is found that these structures typically have a standing capacitance in the region of 10fF. When simulated with a dielectric disturbance above the electrodes, the capacitance is found to change by up to 100%, although a figure of 20% is more usual. However, this change is found to reduce very rapidly as the dielectric disturbance is moved away from the electrode surface. This is illustrated in Figure 3. The height of the dielectric disturbance above the sensor has been normalised to the sensor width.

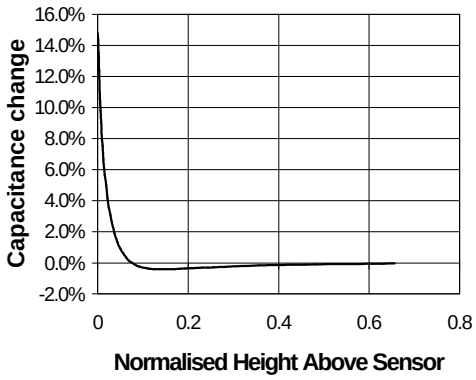

Figure 3: Vertical sensitivity of planar electrodes

Clearly, this rapid drop is a cause for concern. However, this result is derived from investigations of a single dielectric particle.

It can be seen from Figure 3 that the capacitance change becomes negative when the particle is drawn away from the electrode surface. This effect has not been explained, but is believed to be a real effect.

Laboratory scale sensors have been simulated, and the capacitance determined and compared to a real sensor. The results were in good agreement, being within a factor of two of each other. Additionally, the negative capacitance change was confirmed experimentally.

2.2 Requirements for the Measurement Circuitry

Given the size and expected capacitance of the sensors, a different approach needs to be taken to measuring the capacitance than has been traditionally used for macro-scale capacitance tomography. Research in UMIST has focussed on the charge-discharge circuit [3], although AC excited circuits are currently under development [4]. It has been claimed that the charge-discharge circuit can measure capacitances between 0·3fF and 2pF, with a resolution of 0·3fF [5]. Although the capacitance that needs to be measured is within this range, it is at the extreme low end, and the measurement sensitivity is inadequate.

A further disadvantage of the charge-discharge circuit is the circuit footprint. A single charge-discharge circuit has been implemented on custom silicon at UMIST [6]. The resulting chip measures approximately 1.5mm square. It is not feasible to use this much silicon area for one sensing circuit. A tomographic array would require a very large number of these circuits, and would prove impractical due to the large size of

the resultant integrated circuit. A large integrated circuit is disadvantageous as it will be both expensive and have low yield.

Given these problems, it becomes clear that a smaller, more sensitive circuit is required. The circuit needs to have similar dimensions to the sensors, thus allowing integration below the sensors. Additionally, the circuit needs very high sensitivity, with a resolution approaching 10aF.

3 CANDIDATE CIRCUITS

For the reasons outlined above, circuits traditionally considered for electrical capacitance tomography are inappropriate for micro tomography. It is necessary to consider other domains where capacitance measurement is common.

Typical applications of on-chip capacitance measurement are air pressure sensors [7], humidity sensors [8], micro accelerometers [9][10] and manufacturing process characterisation [11],[12].

The air pressure sensor and humidity sensor circuits are inappropriate, as these are large circuits designed to measure a single 'large' capacitance. The measurement capabilities of the micro accelerometers are nearer to the requirements of micro tomography, but these circuits also tend to be very large in terms of silicon area, and are therefore unsuitable. The circuits used for analysing manufacturing processes are the most appropriate. These circuits are designed to measure the stray capacitance between tracks on an integrated circuit. The sensor capacitance that needs to be measured for micro capacitance tomography is analogous to this stray capacitance. A further benefit of these circuits is that they are designed to be incorporated into a variety of chip designs for testing purposes, and are therefore necessarily small.

4 MEASUREMENT CIRCUIT

4.1 Circuit Description

A measurement circuit designed for process characterisation at the University of California at Berkeley [11] has been modified to produce the circuit shown in Figure 4, which is clocked by the signals shown in Figure 5.

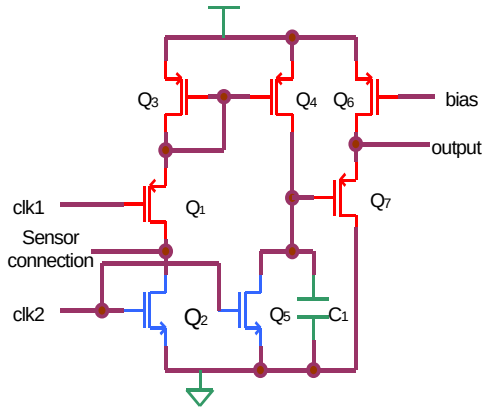

Figure 4: Basic measurement circuit

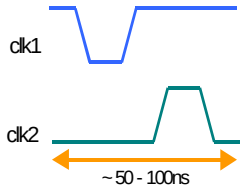

Figure 5: Clocking scheme for measurement circuit

The operation of the circuit is very simple. As clk1 goes low, Q_1 switches on allowing the sensor capacitance, and any associated stray capacitances, to charge to the power supply. The charging current passes through the transistor Q_3, and this current is mirrored in Q_4, which charges a reference capacitor. The voltage across this reference capacitor is proportional to the sensor capacitance and associated strays. The circuit is reset when clk2 goes high.

The current mirror will only behave as expected when the output voltage is lower than V_{DD}-$2V_T$, so care must be taken when selecting C_1 to ensure that this condition is satisfied.

In order to eliminate the effect of stray capacitances, a second, identical circuit is employed. This circuit is not connected to a sensor, and thus the output of this circuit is proportional only to the stray capacitance. The outputs from both these circuits are subtracted using a differential amplifier.

If both circuits are identical and well matched (a common assumption in integrated circuit design), then the stray capacitances should be identical, and should cancel, leaving an output that is purely proportional to the sensor capacitance. This configuration is shown in Figure 6.

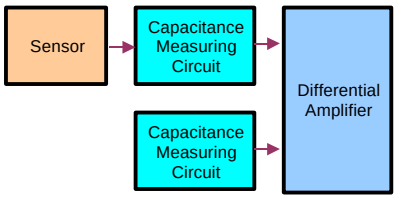

Figure 6: Stray Capacitance Compensation Configuration

Another, potentially more useful configuration is to connect a sensor to both of the circuits connected to the differential amplifier. In this case, not only is the effect of stray capacitance subtracted from the output, but also the standing sensor capacitance. This modified configuration is shown in Figure 7. This configuration is beneficial as it allows the circuit gain to be increased thus allowing small capacitance changes to be measured more accurately. The differential approach is also beneficial for eliminating temperature effects.

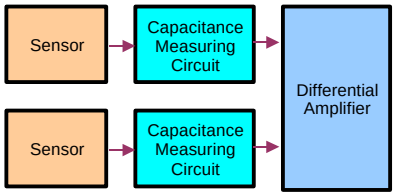

Figure 7: Standing Capacitance Compensation Configuration

4.2 Circuit Analysis

A simplified analysis can be carried out by considering the circuit shown in Figure 8.

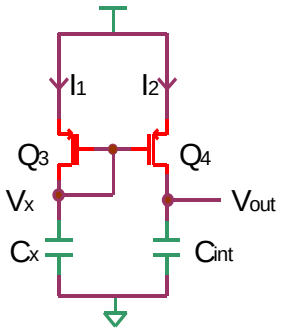

Figure 8: Simplified Circuit for Analysis

This circuit is valid if it is assumed that the switching transistor Q_1 has negligible impedance, and that Q_2 has infinite impedance. In reality, a CMOS transistor that is switched on will have an impedance of the order of kilo-ohms. This impedance will only slow the flow of current into the capacitance, but will not affect the total current flow.

The current through a CMOS transistor is given by equation 1, where μ_0 is the mobility of the charge carriers in the channel, C_{ox} is the gate capacitance per unit area and W/L are the dimensions of the gate.

$$I_{DS} = \frac{m_0 C_{ox} W}{L}\left[\left(|V_{GS}| - |V_T|\right) - \frac{V_{DS}}{2}\right] V_{DS}\left(1 + l V_{DS}\right) \quad (1)$$

If the effect of channel length modulation is ignored, and noting that Q_3 is saturated, equation 1 simplifies to the expression in equation 2.

$$I_{DS} = \frac{m_0 C_{ox} W}{2L}\left(|V_{GS}| - |V_T|\right)^2 \quad (2)$$

Ignoring the effects of channel length modulation simplifies the model, allowing analytical solutions for the transistor currents.

The effects of channel length modulation are only important in current mirrors when the drain-source voltages of both transistors are significantly different [13]. In this case, they are broadly similar, as both capacitors in the circuit will charge at a similar rate.

The current flowing through Q_3 is the charging current for C_x. This current is related to V_x by equation 3, and when solved this yields equation 4.

$$V_x = \int_0^t I_{DS}\, dT \quad (3)$$

$$V_x = \frac{\left(\frac{m_0 C_{ox} W_3}{L_3}\right)\left(V_{DD} - |V_T|\right)^2 t}{2C_x + \left(\frac{m_0 C_{ox} W_3}{L_3}\right)\left(V_{DD} - |V_T|\right) t} \quad (4)$$

If the current mirror is operating as expected, then Q_4 will also be in its saturated mode of operation. Therefore, equation 4 can be applied in equation 2 to give an expression for the output voltage as shown in equation 5.

$$V_{out} = \frac{L_3 W_4}{W_3 L_4}\frac{\left(V_{DD} - V_T\right)}{C_{\text{int}}}\left[1 - \frac{1}{1 + \frac{1}{C_x}\left(\frac{m_0 C_{ox} W_3}{2L_3}\right)\left(V_{DD} - |V_T|\right) t}\right] C_x \quad (5)$$

The output voltage settles to the value given by equation 6.

$$V_{out} = \frac{L_3 W_4}{W_3 L_4}\frac{\left(V_{DD} - |V_T|\right)}{C_{\text{int}}} C_x \quad (6)$$

When two of these circuits are combined and their outputs subtracted with a differential amplifier with a gain K, the output is given by equation 7, where C_{x1} and C_{x2} are the capacitances connected to the measuring nodes.

$$V = K\frac{W_3 L_4}{L_3 W_4}\frac{\left(V_{DD} - |V_T|\right)}{C_{\text{int}}}\left(C_{x1} - C_{x2}\right) \quad (7)$$

If the circuit is operated with one sensor in the stray capacitance compensation configuration shown in Figure 6, then the output voltage is given by equation 8.

$$V = K\frac{W_3 L_4}{L_3 W_4}\frac{\left(V_{DD} - |V_T|\right)}{C_{\text{int}}} C_{sensor} \quad (8)$$

If the standing capacitance compensation configuration shown in Figure 7 is employed, the output will nominally be zero, with a change in capacitance in either sensor, ΔC, causing an output voltage given by equation 9. (The sign will be positive or negative, depending on which sensor is disturbed.)

$$V = \pm K \frac{W_3 L_4}{L_3 W_4} \frac{\left(V_{DD} - |V_T|\right)}{C_{\text{int}}} \Delta C \quad \textbf{(9)}$$

If ΔC is a small proportion of the standing capacitance, it can be seen from these expressions that the system gain can be set higher without saturating the circuit when the standing capacitance cancelling configuration is used. This allows for a more sensitive configuration. Clearly, this structure is only useful if only one sensor is disturbed at any given time.

4.3 Simulation Results

Simulations were carried out using a SPICE circuit simulator. The simulations were carried out on a layout of the circuit for a 0·8μm CMOS process. In all cases, the circuit was simulated in the standing capacitance configuration (a standing capacitance of 10fF was assumed).

Figure 9 shows the charging waveform of the sensor capacitance.

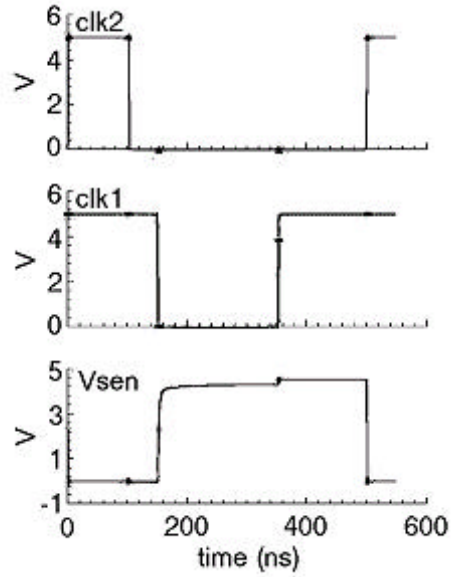

Figure 9: Sensor Capacitance Charging Waveform

The final value for the voltage across the capacitance is in good agreement with equation 4, but the time relationship is not. This is due to the assumption that the on resistance of Q_1 (Figure 4) is zero. This is not true in reality, thus the derived equation does not take into account the effects of the series resistance on the transient response.

The output voltage of the differential amplifier in response to a change in the capacitance of one of the sensors is shown in Figure 10 and Figure 11. The capacitance of one sensor was kept constant at 10fF, and the other varied between 8.6fF to 11.4fF. The differential amplifier gain was 25, the reference capacitor was 60fF, and the current ratio of the current mirror was unity. The system was clocked at 2MHz.

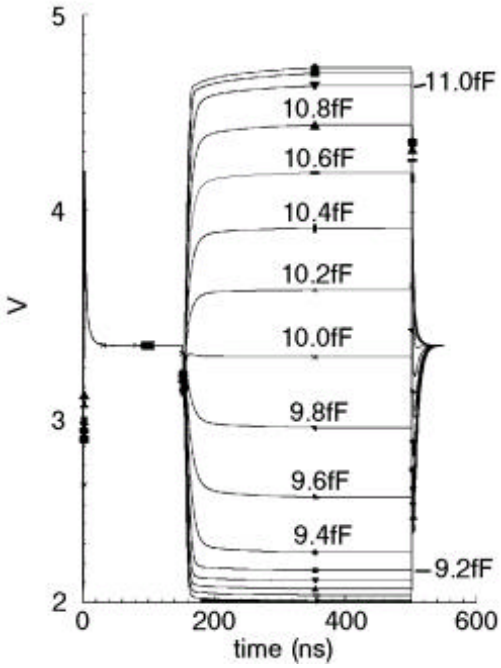

Figure 10: Output Voltage of Differential Amplifier as Sensor Capacitance Varies

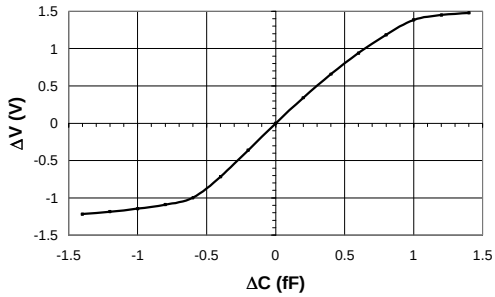

Figure 11: Sensor Response to Varying Capacitance

Figure 11 shows that the circuit is reasonably linear when the capacitance change is between -0·6fF and 0.9fF. The non-linearity for larger capacitance changes is due entirely to the differential amplifier. It can be seen in Figure 10 that the circuit settles very quickly, and thus operation at higher frequencies than 2MHz may be possible. However, it is likely that the factor that most limits the operating frequency will be the electronics driving the signals from the chip.

From Figure 11, we can see that the measurement sensitivity in the linear region is approximately 1.6 V/fF. This can be compared to the sensitivity predicted by equation 9. Given the gain of the differential amplifier and the capacitance of the reference capacitor, and assuming a nominal value for V_T of 0·8V, the predicted sensitivity of the circuit is 1.75 V/fF, which is in good agreement with the simulation result

4.4 Design Considerations

When implementing the circuit, special care must be taken when creating the layout. There are several parameters that must be well

matched in order for the circuit to be implemented successfully.

With reference to equation 7, it is seen that there are several parameters that must be matched between both differential arms of the circuit.

The current mirrors must both be matched to each other in two respects – geometrically, and physically.

Geometrical matching is governed by the mask that defines the transistor gate. This may be improved by using transistors that are at least double the size of the minimum allowed, and by aligning the transistors on the same axis.

Physical matching depends on the carrier mobility, the gate capacitance and the threshold voltage. The mobility and threshold voltage are dependent on the doping of the channel. The gate capacitance depends on the local thickness of the oxide that insulates the gate from the channel. Both doping and oxide thickness can be matched by placing the transistors in close proximity to each other.

The reference capacitors must also be well matched. Capacitors are formed on an integrated circuit by overlapping two layers of polysilicon separated by a thin layer of silicon dioxide. The matching is governed by geometrical considerations.

Good geometrical matching of capacitors is achieved by using regular structures as shown in Figure 12.

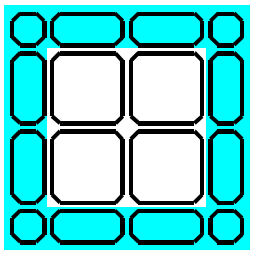

Figure 12: Dummy Structures for improved Matching

This figure shows four matched capacitors. Other features of this layout are the use of dummy capacitor structures (shown shaded) in addition to the active capacitors, and 45° corners on all features.

Another important factor is whether the stray capacitance is sufficiently similar in both circuits to cancel each other out. This is largely dependent on the geometrical matching of the transistors in the circuit, and mismatch will be minimised by avoiding the use of minimum size transistors.

4.5 Prototype Circuit

A prototype integrated circuit has been manufactured using a 0·8μm CMOS process. The integrated circuit incorporates several large arrays of capacitance sensor. The layout of one of the arrays on the integrated circuit is shown in Figure 13.

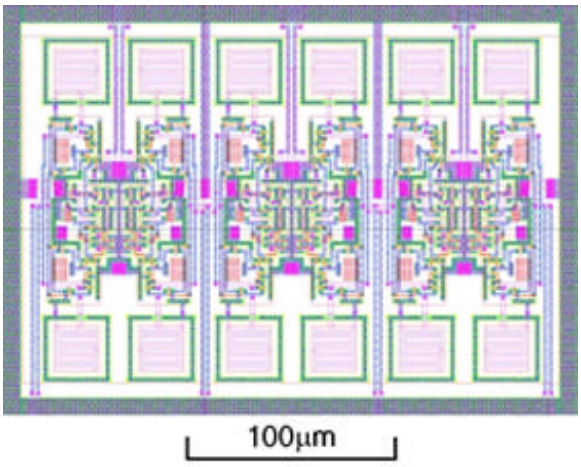

Figure 13: Layout of a 12 Sensor Array

This array contains six pairs of electrodes (top and bottom). Each pair is monitored by a single set of circuitry to form the standing capacitance compensation configuration. The layout of the sensor circuitry, for each 'channel', measures ≈ 100μm × 25μm. The circuitry was not integrated below the electrodes in this prototype as there were only two metal layers available in the process used.

There are sixteen arrays on the integrated circuit in total, each containing various sensor configurations and gain settings. The performance of the various sensor/gain combinations will be initially be evaluated by placing dielectric objects above one row of sensors. If these tests are positive, the integrated circuit will be tested in a flow rig.

5 CONCLUSION

A circuit has been presented that has potential for use in micro-capacitance tomography. The circuit has been analysed, and shown to work by simulation. A prototype integrated circuit has been designed containing several of these circuits and will be evaluated to confirm that this circuit is viable. Once proven viable, this circuit will be applied to a linear micro-tomography system [14].

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