A Microcontroller-based High-speed Serial Link For Process Tomography Systems

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Abstract *- A process tomography system usually employs a PC for operation control and image reconstruction. The on-line image reconstruction speed is mainly limited by data acquisition and image reconstruction processes. An intelligent interface has been developed with a microcontroller, Transputer link adaptor chips (C011) and optical fibres to perform data acquisition, so that the PC CPU can be dedicated to image reconstruction. The interface card is embedded in the PC as the host terminal of the link. A C011 in the other terminal is configured to have two 8 bit parallel ports (one input and one output) for interfacing with sensing circuits. The microcontroller receives commands from the PC and controls data acquisition processes. Data sent by the distant terminal is collected by the microcontroller and stored in memory on the card. Once a set of data for one image has been collected, it is uploaded to the PC. It has been successfully applied in an electrical capacitance tomography system.*

Keywords: Data transmission, Microcontroller system, PC interface, Capacitance tomography

1. INTRODUCTION

Process tomography (PT) is a technique of obtaining images of a cross section of an industrial process, e.g. a multi-phase flow in an oil pipeline, so that the internal behaviour can be investigated [1]. A PT system consists of three main units: (1) sensor unit (2) sensing electronics unit and (3) image reconstruction unit. The sensor is mounted directly onto the process equipment and the sensing electronics is located at the site of measurement. The image reconstruction computer may be located far away from the process, e.g. in the central control room, as the site may be hazardous. A PT system is capable of producing tens to hundreds of images per second, which requires a high-speed serial link, say 20 Mbits per second.

At UMIST, two types of electrical capacitance tomography (ECT) systems have been developed, i.e. Transputer-based system and PC-based system. The Transputer-based system employs five Transputers (T1-T5) [2]. Data acquisition tasks are performed by T1. T2 and T3 are dedicated to image reconstruction. T4 acts as an interface to PC and T5 is a graphics processor. This system can do on-line image reconstruction at 40 frames per second. However, the cost of the Transputer array hinders the commercialisa-tion of the system.

The PC-based system has been developed as an alternative to the high-cost Transputer-based system. The PC performs both data acquisition and image reconstruction. As an RS232 serial port has neither an enough speed nor driving capability, a dedicated C011-based interface card has been designed to serve as a high-speed serial link. Without the Transputer array, the system has a reduced on-line image reconstruction speed of about 10 frames per second. In the PC-based system, bulk of the PC CUP time, about 50%, is spent on data acquisition, because the PC CUP has to visit the C011 for every byte of data, 128 times for a 12-electrode system. In fact, the time for data acquisition can be released and used for image reconstruction. A solution is to use a dedicated microcontroller with RAM to perform data acquisition and let the PC mainly do image reconstruction. This paper describes an interface card developed with a micro-controller (8051) and a C011 to perform data acquisition.

2. GENERAL DESCRIPTION

8051 is a general-purpose 8-bit micro-controller, which is compatible with PC architecture and other common logic devices. The chip has four bi-directional 8-bit input/output ports. Port 0 functions as a multiplexed data/address bus. The direction of data flow is programmable by software. The microcontroller is capable of accessing up to 64 Kbytes of external

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memory. It allows two external interrupt lines to be connected [3-5].

C011 is a serial link adaptor designed for the use in Transputer systems. It provides full duplex communication between two entities. Primarily, it functions as a parallel-to-serial & serial-to-parallel converter. The link adaptor can operate in one of two modes:

Mode 1: two 8-bit parallel ports (one input, one output) with full handshake signals
Mode 2: one 8-bit bi-directional port with memory-mapped registers and inter-rupt signals.

C011 communicates at either 10 or 20 Mbits/sec [6]. Besides used in Transputer systems, it also supports sub-system architecture in non-Transputer applications. A serial link can be set up by connecting two C011 chips back-to-back as shown in Fig.1.

The designed serial link includes three main units:

(1) a PC interface card with an 8051 and a C011 operating in Mode 2, which is embedded in a PC at the local end, i.e. microcontroller-based interface circuit
(2) a terminal board with C011 operating in Mode 1 at the remote end
(3) serial link wires which can either be optical fibres or coaxial cables

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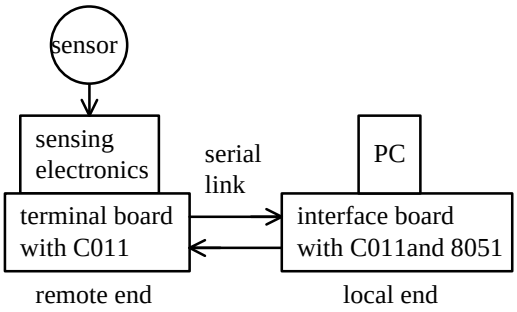

Fig.1 PT system with two C011s at both ends

Fig.2 depicts the interface card operation in chronological order. Initially, the user chooses data acquisition or image reconstruction. The PC sends a pre-defined command to the microcontroller on the card. The microcontroller starts to execute the data acquisition program in its ROM. It co-ordinates the control activities of both C011 and the external memory. The microcontroller sends out commands via C011 serially. In response, the sensing electronics unit sends back a two-byte measurement. The data is written into the external memory. A total of 128 bytes of data are received to contribute to an image for a 12-electrode system. Once a set of measurements is collected for one image, the microcontroller up-loads the data to the PC for image reconstruction. While PC reconstructs the image, the interface card initiates data acquisition for another set of image data.

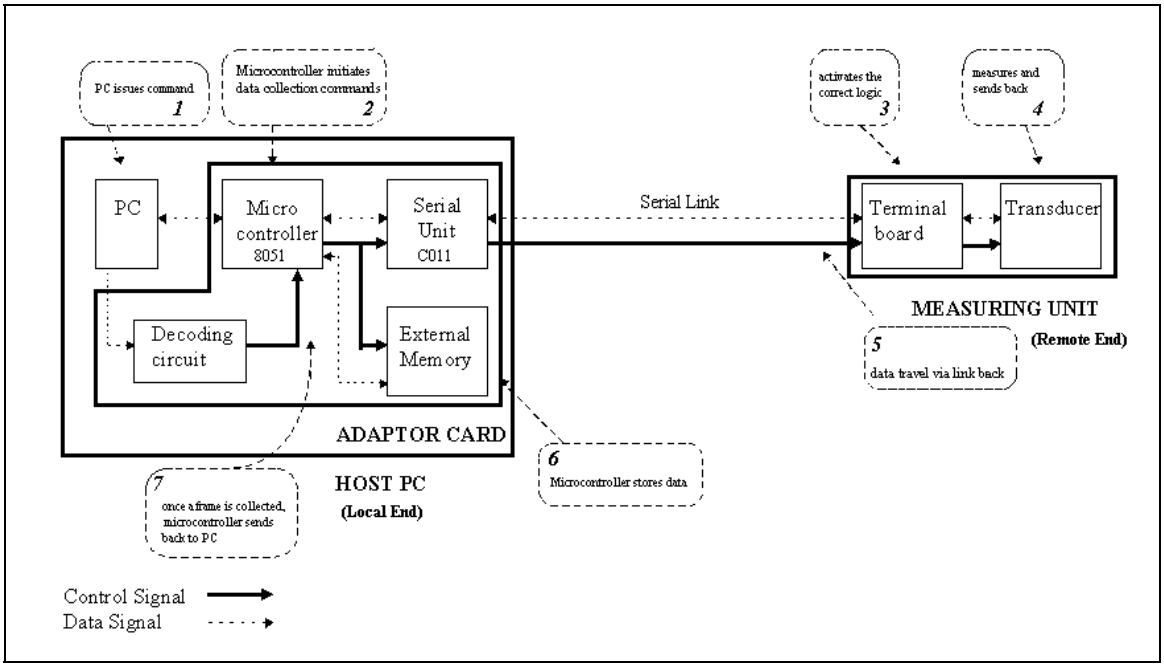

Fig.2 Control and data flow chart of the microcontroller-based interface card

3. CIRCUITS

3.1 Microcontroller-based interface circuit

The circuit of the microcontroller-based interface card is depicted in Fig.3. Port 1 of 8051 is connected to the PC data bus SD0-7 via a bus transceiver (74LS245). The address decoding circuit consists of an 8-bit magnitude comparator (74LS688), three OR gates (74LS32), an AND gate (74LS08) and an inverter (74LS04). It allows access to the interface card, only when the address on the PC address bus matches those pre-encoded by four DIL switches (A2-A5). In addition, it ensures the correct direction of data flow and alerts the microcontroller via its interrupt request line (INT1) during RD or WR. Fig.4 illustrates the timing for the PC and the microcontroller during RD and WR [7]. P3.5 of 8051 is used to alert the PC when microcontroller has data for uploading. PC interrupt request line is selectable through four DIL switches. Port 0 serves as the multiplexed address/data bus of 2 Kbyte external memory. It is connected to the low-byte address of the memory via a data latch (74LS373). The upper address bits (A8-A10) are controlled by P2.0-P2.2. RD and WR signals are controlled by P3.6 and P3.7, respectively.

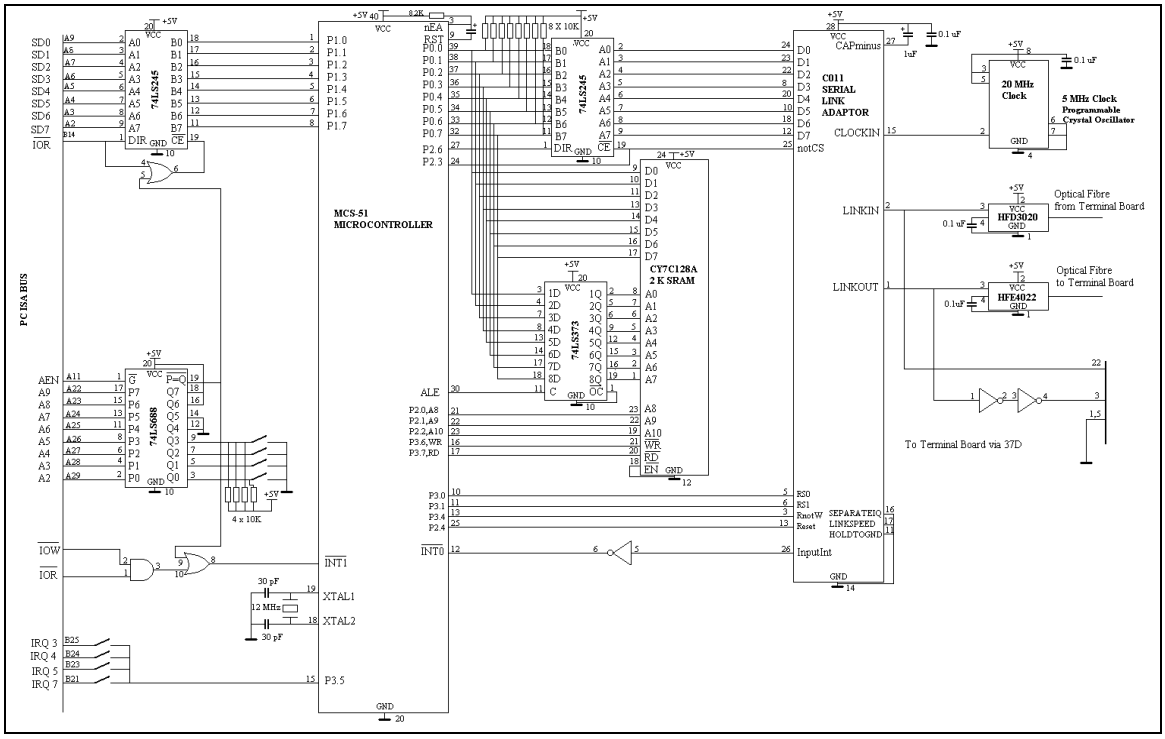

Fig.3 Microcontroller-based interface circuit.

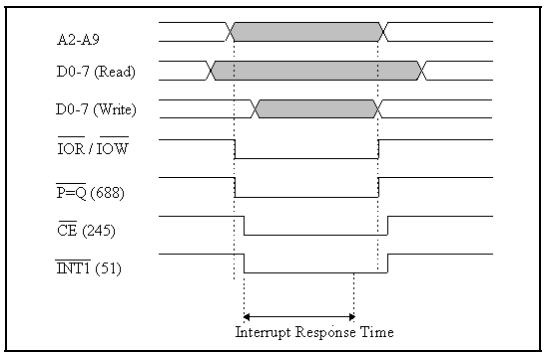

Fig.4 Timing diagram of microcontroller-based interface card

The C011 on this card operates in Mode 2. Port 0 also serves as the data bus of the C011, connected via a bus transceiver (74LS245). The chip select signals are controlled by the microcontroller through P2.3. Direction of data flow is ensured by P2.6. The link adaptor can transmit data electrically through a double hex inverter. It can also transmit and receive data optically through transmitter (HFE 4022) and receiver (HFD 3020), respectively. When a byte of data is received, C011 alerts the microcontroller by asserting interrupt request (INT0).

3.2 Terminal board with two parallel ports

C011 at the other end operates in Mode 1 [8]. The block diagram is depicted in Fig.5. A unique RESET signal is needed as illustrated in Fig.6 [6].

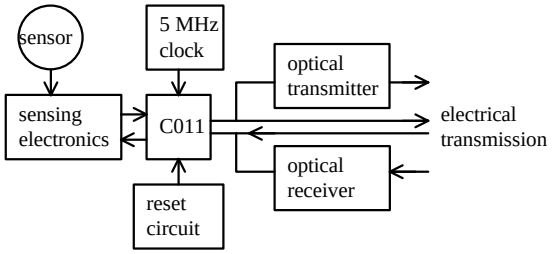

Fig.5 Terminal board with two 8-bit parallel ports

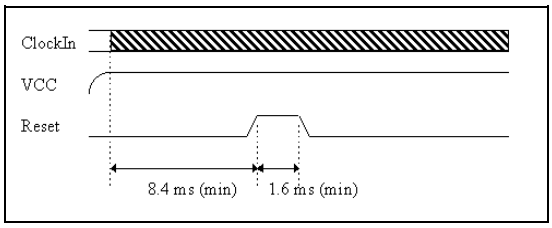

Fig.6 C011 RESET

4. INTEGRATION INTO UMIST ECT SYSTEM AND EXPERIMENTAL RESULTS

The software was written in Intel assembly language and downloaded to the ROM of 8051. The microcontroller obeys the PC and commands the distant sensing electronics to obtain a set of data for an image by executing the data acquisition program. It also implements a half duplex communication between the microcontroller and the PC. This enables the microcontroller to upload measurements to the PC. The functions are achieved through several essential modules: (1) initialisation of C011 (2) data transmission via C011 (3) data reception via C011 (4) data acquisition algorithm and (5) reading or writing to the PC.

Prior to integration into the UMIST ECT system, the interface card was tested for functionality. The hardware modules tested were: (1) microcontroller (2) microcontroller and external RAM (3) microcontroller and C011 link adaptor and (4) decoding circuits.

The card was embedded in the ECT system developed in 1995 [2]. The link between the PC and the sensing electronics was checked by selecting one electrode as an excitation electrode. The signal is depicted in Fig.7.

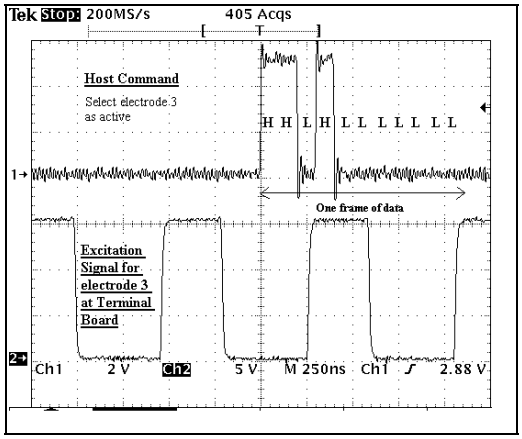

Fig.7 Excitation signal on electrode 3

The command to start data acquisition was sent from the PC to 8051. At any time, only one electrode should be active and measurements in 2 bytes were taken from another electrode. The sensor with electrodes symmetrically mounted outside was firstly emptied and then filled with plastic beads. For empty, low magnitude readings were obtained, whereas the filled sensor gave high magnitude readings. Two typical measurements are depicted in Fig.8 and 9.

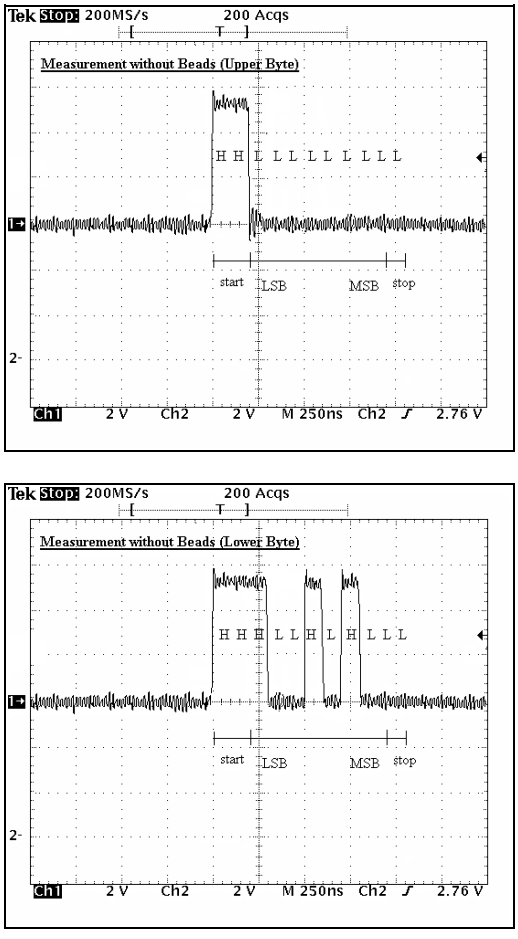

Fig.8 Two-byte measurement from the electrode with the pipe emptied

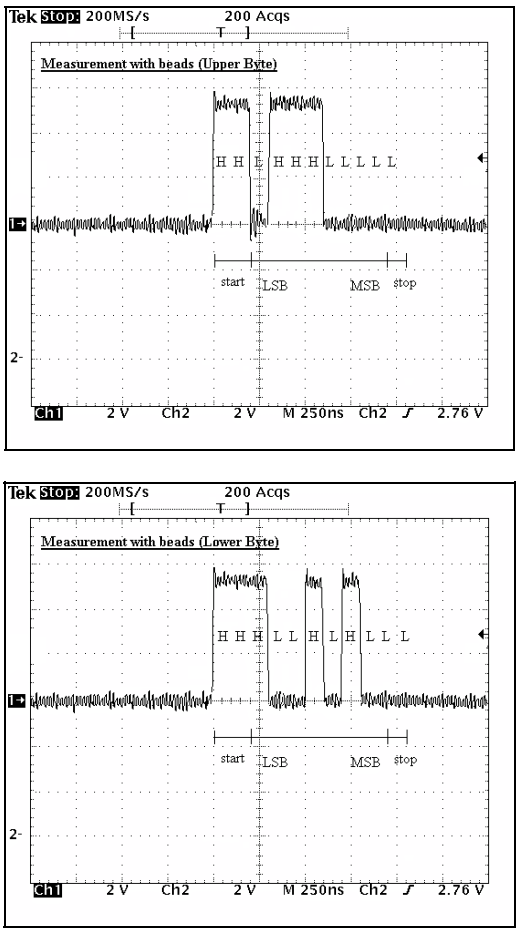

Fig.9 Two-byte measurement from the electrode with the pipe filled with beads

The data acquisition program illustrated in Fig.10 was executed to confirm the time spent on data acquisition. The inner loop of instructions were executed by the micro-controller with C011 input and output signals observed. The response time for a single measurement is approximately 10.4 μs, as can be seen in Fig.11.

The time to reconstruct one image was measured to be approximately 8.48 ms using CLOCK function in C. The time taken by the microcontroller to upload a set of measure-ments (128 bytes) was measured to be 0.33 ms. Therefore, the total PC CUP time for one image would be 8.81 ms, resulting in an on-line image reconstruction speed of 110 frames per second. This is a significant increase, compared with 40 frames per second for the Transputer-based system and 10 frames per second for the PC-based system. With the microcontroller based interface card, the PC CUP can be fully dedicated to image reconstruction while the data acquisition tasks are carried out by the microcontroller.

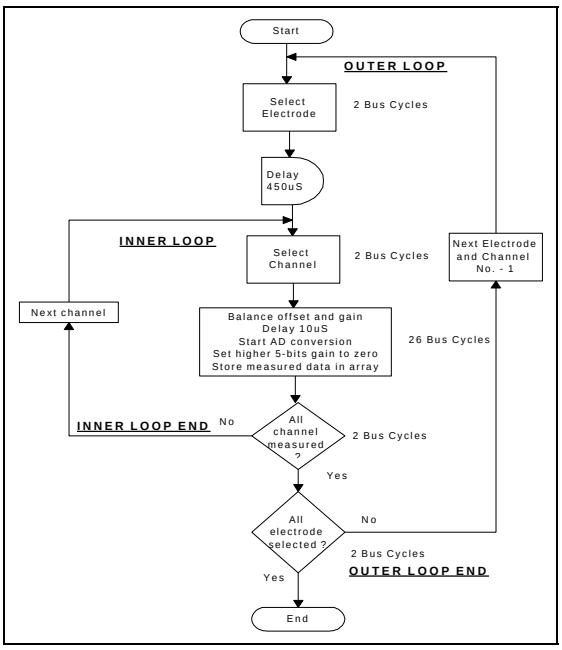

Fig.10 Flow chart of data acquisition

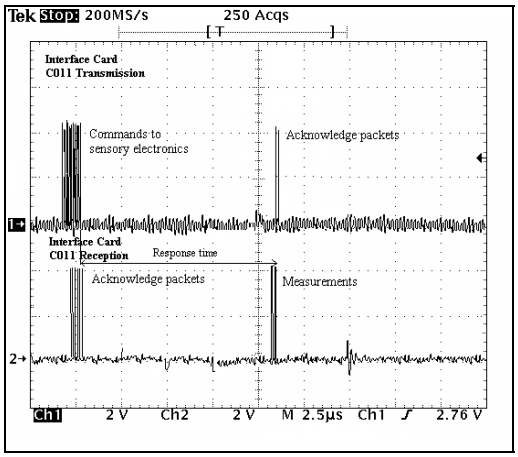

Fig.11 Single channel measurement

5. CONCLUSION

Approximately, half of the PC CPU time is used in data acquisition in the PC-based ECT system with a simple interface card. A microcontroller-based interface card has been developed to release this time. The card has been tested successfully, achieving significant improvement in on-line image reconstruction speed. The use of inexpensive components in this design makes the interface card cost-effective and commercially viable.

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