Multi-Sensor Process Tomography System Design: Part 1 – Systems and Hardware Engineering

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Abstract *-- This paper deals with the conceptual design of an integrated multi-modal system which can offer a 'plug and play' capability. It deals with the design constraints of such systems: the complexity and specificity of the front end electronics for each modality; the need for front end data pre-processing and packing; the need to integrate the data to allow data fusion; and finally the features to enable successful data fusion and interpretation. This paper, Part 1, focuses upon the composite systems engineering and integrated hardware. A further paper, Part 2, deals with the data processing and system software design.*

Keywords: multi-sensor tomography, multi-modal tomography, data fusion

1. MULTI-SENSOR TOMOGRAPHY

Many target processes for which tomography offers a potential valuable insight are complex and involve multiple components. Because of their complexity such process are likely to be operated purely through empirical information, gathered over many years. Although such systems and their operations may be efficient and productive, the lack of knowledge of the internal behaviour may impose a serious constraint, both upon the design of new plant and upon the flexible operation of existing plant.

The use of process tomography has been shown to offer a new insight into a number of processes. Its power is potentially multiplied when several tomographic modalities can be used concurrently.

Such joint use demands the need for data fusion in order to deliver an integrated result. Current generation PT systems are complex, expensive and have been designed primarily for the prototype laboratory. In order to effectively deploy multiple sensors a system must allow their individual data to be collected efficiently and combined effectively. There are opportunities both for rationalisation and sharing of resources and hazards of mutual interference.

2. SYSTEMS ENGINEERING DESIGN

A group of logical system elements are first proposed based upon a simple set of assumptions or basic design parameters.

2.1 Basic design requirements

- Multi-sensor design: support for individual sensor front-end buffering and control electronics to optimise the location of each sensor modality to its ideal physical location on the process of interest.
- Data acquisition and processing: to offer distributed appropriate sensor-head processing, but to provide common 'plug and play' sensor data acquisition allowing flexible fusion at all relevant points.
- Systems integration: capable of scaleable implementation, from experimental test-bed to harsh industrial setting in compliance with intrinsic safety and EMC standards; to exploit standard sub-systems where appropriate.
- Interpretation and exploitation: to facilitate usage of final reduced data for flexible range of monitoring and control applications.

These requirements have been realised in the following implementation.

2.2 Outline design and standards

Before embarking upon a detailed hardware and software design a range of Systems Engineering and Data Standards were agreed by the team. Although some of these have not been realised in the final implementation, they have been very useful in segmenting the design effort between members of a large team.

A typical multi-mode system to the above requirements could comprise:-

- several Sensor Sub-systems (S-S) which offer their status and data information on demand;
- a (potentially long) link from each sensor sub-system via a Sensor Communication Sub-system (SC-S);
- a Data Acquisition Sub-system (DA-S) which gathers data from all sensors through the SC-S and provides simple signal processing, for example to provide filtering to reduce noise etc.;
- a Sensor Data Layer (SD-L) which defines the format of all signals and messages in the link between each S-S and the DA-S;
- a Processed Data Layer (PD-L) which offers direct access to the collected data from each sensor, including appropriate timing information - this layer is intended for experimental use to allow analysis etc by external software and hardware;
- a Reconstruction Sub-system (R-P) which takes the processed sensor data and provides the necessary tomographic reconstruction;
- an Intensive Processing Sub-system (IP-S) which, when required, can provide increased processing to provide real-time capabilities;
- the Raw Image Layer (RI-L) offering direct access to the internal images produced from the reconstruction processing - allowing examination with external software tools such as AVS;
- a Data Fusion Sub-system (DF-P) which allows the combination of the multiple sensor data to reveal super-data-set features which may be interpreted in terms of the user process;
- an Interpretation and Feature Fusion Layer (IFF-L) provides a common format in which to offer derived data to be passed to other systems, or logging systems;
- a Configuration and Control Program (CC-P) which offers configuration services to the user (for experimental implementations); integrates the various functions; and delivers the requested outputs.

Figure 1 shows the schematic arrangement of these sub-system and data layers.

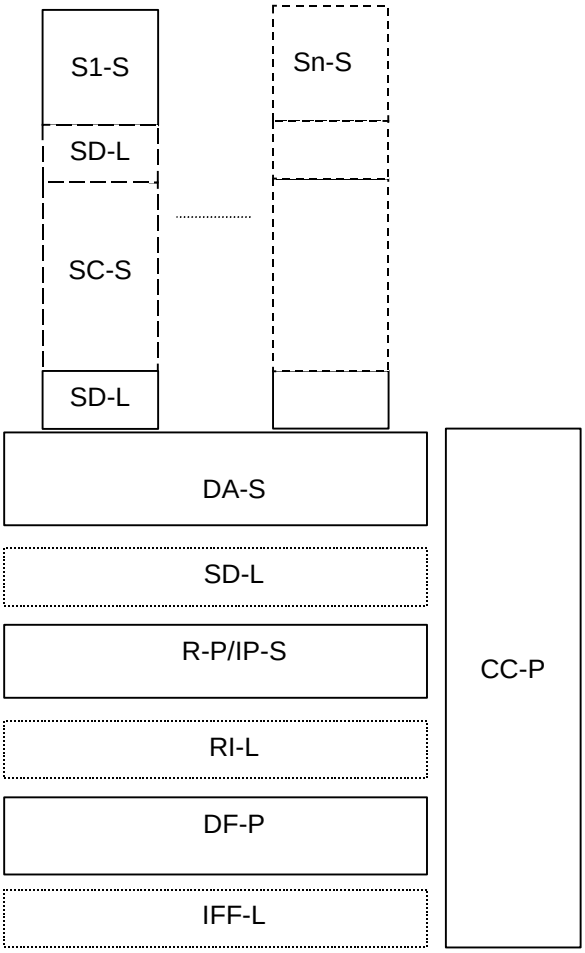

Figure 1: Outline System

2.3 Sensor sub-system requirements

Each sensor type will have both general and specific control and monitoring parameters. In this case these are assumed to be as tabulated below. The list is restricted to low cost sensors that operate predominantly through electrical interactions, although other types could be introduced with appropriate front-end sub-systems. These parameters are:

General
- Number of planes
- Number of electrodes / transducers per ring
- Data format
- Sensing configuration (slightly different for each modality)
- Measurement resolution

Electrical resistance tomography (ERT)
- Current
- Frequency
- Signal phase shift
- Gain map
- Sampling number

Electrical capacitance tomography (ECT)
- Frequency
- Phase adjustment

Ultrasound sensor tomography (UST)
Amplitude and time of flight data
Pre-amplifier gains
Diagnostic data on faulty transducers

3. SYSTEM IMPLEMENTATION

Implementation issues of the hardware sub-systems offer a range of options. Those having general design interest are reviewed below. Processing details are discussed in detail in the second part of this paper [1].

Each sensor subsystem (S-S) will need appropriate analogue circuitry to deal with the sensor control and data signals. Resulting data will be converted to digital format and transmitted via the SC-S physical link to a composite multi-sensor data acquisition DA-S and processing sub-system.

The link should be standard so that any S-S link can be 'plugged into' the host instrument. This would interrogate the S-S which would respond with its sensor type, how many sensing elements it has, how many planes, etc.

To permit this 'plug and play' sensor to interact to these queries, and to allow pre-processing, it is convenient to provide a small processor or micro-controller on the sensor subsystem. The hardware items that need to be standardised with this configuration are the processor and the host link.

The simplest realisation for the data acquisition and processing sub-systems is an appropriate personal computer, equipped with a current fast (PCI) bus. For implementations in which specific functionality is embedded, for industrial end-use rather than an experimental trial, a purpose designed unit having ROM-based software could be employed.

The following review provides more details of key design aspects.

3.1 Sensor sub-system, S-S

Since the S-S deals with specific sensors its internal form will be dictated by the requirements of each sensor type. It is clear that the front-end analogue electronic control and data interfacing must be specific to each type. However apart from these front-end components, all other hardware may be generic. Variations can be dictated by software.

The sub-system will be expected to include its own power supplies allowing a distributed realisation and removing any need for the host data acquisition and processing instrumentation to pass power to its sensor outstations.

It must also provide control and data signals as specified to the SD-L. Since the SD-L is specified to deal with only a single sensor modality, this sub-system cannot itself combine sensor data capture for multiple modes.

The S-S unit in schematic form is shown in Figure 2.

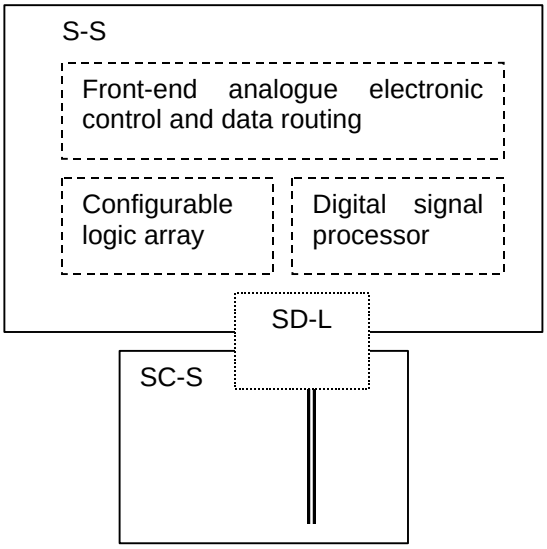

Figure 2: Schematic sensor sub-system

As discussed the front-end electronics provide the minimal specific support for the sensor type, for example the current drivers and detectors for an ECT system. The analogue electronics are controlled by a generic (software) configurable logic array. An Altera device has been used in developmental systems.

For simplicity of design it is convenient to standardise upon a common arrangement of logic array and digital signal processor (DSP) for all sensor type S-S units.

The DSP provides logical message-based communications with the host data acquisition system, via the SC-S. Hence it must be able to cope with the most demanding sensor type in terms of pre-processing and data buffering. The UST subsystem must perform extensive data pre-filtering and conversion and has therefore been used as the speed benchmark.

A range of possibilities were considered including small 8-bit micro-controllers such as the 8051 or the 68HC11. Evaluations indicated that these would not be fast enough to support current UST needs.

The processor selected based upon previous trials is an Analog Devices low cost DSP (part number ADSP-2181), which could be later upgraded to a ADSP21061. This has 1Mbit of on-chip memory and SHARC ('Super-Harvard' - separate program and data bus) architecture. Conveniently the device also offers a C-compiler allowing high-level language software development.

The generic electronics of the S-S unit consists primarily of the Altera and the Analog Devices DSP chips plus other minor devices.

The software configurable Altera device, in effect, provides the 'glue logic' to interface and drive the specific analogue front-end electronics for the sensor.

The sensor head part of the serial communication channel (the SC-S) is implemented on the same unit as the S-S. As discussed in more detail below, this is realised through a simple 'daughter board' to allow this sub-system to replaced completely by other candidates offering higher speed or more appropriate industrial performance, for example optical fibre drivers. This provides the core requirement of scaleability to an industrial trial in which intrinsic safety and EMC standards exist.

3.2 Sensor communication sub-system, SC-S

This sub-system provides the channel through which the sensor sub-system can offer data on demand from the Data Acquisition Sub-system.

For practical reasons a serial implementation is potentially attractive based upon the requirements noted, where the sensor head and the following processing sub-systems may be separated. Further where high noise or intrinsic safety requirements exist the possibility of optical fibre implementation is attractive. Several viable technology options were considered for serial data transfer, where they may offer a useful combination of high speed and standard accessible technology.

For simple peripheral connection in small computer systems the Universal Serial Bus (USB) is gaining in popularity. This has a maximum speed of 12Mbits/s (1.5 Mbytes/s) but has some control overheads and a more realistic data transfer speed would be below 1Mbyte/s and thus is too slow for this application.

Another interesting recent standard is the IEEE 1394 (or *Firewire*) communications system which offers speeds of 100-200Mbits/s (12.5-25Mbytes/s). An example is an Adaptec PCI card (AHA-8940), which offers 3 Firewire ports. This card could provide 3 S-S 'plug and play' ports, probably sufficient for many PT systems. A further possibility is to use the physical link chip (PHY) used in the cards that support the IEEE 1394 standard and build the communication around this chip without out having to adhere to the logical protocols of the standard.

A further option considered is the use of the Inmos *transputer* link chip (IMS-C011) which operate at 20Mbits/s (1.8Mbytes/s). The design team had experience in their use for both ECT and UST system. A further option was the use of the link chip for the T9000 transputers that offers 100Mbit/s. The IEEE 1355 standard defines this system.

Table 1 below summarises the options and typical part details.

Speed (Mbit/s)	Standard	Chip/Card-set
Sensor end		
20	OS-link	Inmos C011- 28pin SOJ/DIL chip
100	IEEE 1394 Firewire…	TI TSB11C01 DL 56pin SSOP chip (PHY_layer)
100	…IEEE 1394 Firewire	TI TSB12C01A PZ 100pin TQFP chip (LINK_layer)
100	IEEE 1355 DS-link	SGS STC101 F10S 100pin CQFP chip
Host end		
20	OS-link	Inmos C011- 28pin SOJ/DIL chip
100	IEEE 1394 Firewire	TI TSBKPCITST PCI card with 3 links
100	IEEE 1394 Firewire	Adaptec AHA-8940 PCI with card-3 links
100	IEEE 1355 DS-link	STC101 -F10S 100pin CQFP chip
	PCI-bus	AMCC S5933 PCI 160pin PQFP chip
	PCI-bus	AMCC matchmaker PCI evaluation kit

Table 1: Overview of SC-S link options

A further attractive option was the use of a 100Mbit/s Ethernet link. Several chipsets were identified and numerous cards are available for the (PCI-bus) host side of the link. However for the other side of the link (sensor subsystem) no products were found which could be easily interfaced and hence this is not included in the table.

The host interface is mainly determined by the chosen link standard. In the simple experimental implementation it is possible to build an ISA or a PCI-bus interface card. The ISA (AT-bus) would be simple to implement, but has a major speed limitation of about 5MByte/s. The PCI-bus offers a theoretical limit of 132MByte/s. As noted in Table 1, available chipsets/cards offer a relatively easy interface to the PCI-bus.

The various technical and previous experience aspects were considered in order to choose the most appropriate solution for an initial experimental system. The transmission speed of current ECT and UST subsystems is 20Mbit/s using CO11 chipsets. This is adequate for the current requirements, although near the usable limit for the UST system. The USB is too slow and IEEE1394 is fast but unproven and may be difficult to implement. The 100Mbit/s Ethernet option was attractive but although the fast chipsets were available, building an Ethernet

card with high-speed design rules and writing the software to comply with the transport protocols was considered too time consuming in this project.

For reasons of simplicity and ease of design reasons the CO11 chip working at 20Mbit/s was adopted. In order to allow later upgrading of the processor board on the sensor end, this was implemented as a separate 'daughter board' module. A PCI board was designed and constructed for the PC end of the SC-S. This PCI board provides four CO11 channels and a small amount of processing power. The overall design allows the whole SC-S to be replaced with an alternative option, either to take advantage of new technology or to permit the simple use of an SC-S designed to comply with industrial needs.

3.3 Data acquisition sub-system, DA-S

This sub-system provides timed data requests to each SC-S and receives the results. It may also offer a small range of 'in-line' processing, such as digital filtering to remove noise, etc. It provides the platform on which the various layers and processing stages are implemented in software using the host processor, unless an intensive processing sub-system IP-S, is installed.

For the system designed for experimentation this is implemented through the use of a PCI-bus based personal computer. No special features are needed but clearly the ultimate sampling and processing capability will be limited by the processor and associated memory and disk speeds and the facilities provided by its operating system.

3.4 Intensive processing sub-system, IP-S

A variety of attractive candidates are available from current technology. This will undoubtedly be an area in which rapid developments will be made and one in which it is prudent to choose a system which is readily available; offers current frontline performance, and supports portable software. Ideally the system should offer scaleable processing with good software development support to permit tomographic and data fusion software to implemented using this additional processing resource.

The ADSP-21060 (SHARC) was considered as a primary candidate. This high speed DSP processor probably represents the state of the art and offers multiple links for parallel use. PCI-bus cards are readily available with multiple SHARCs on board, supported by portable software tools.

The ARM processor is a further option. It has sufficient processing power and a large memory addressing space.

An IP-S is not included in the experimental system constructed to date.

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